

## In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

- 1 1. (Currently Amended) A multiply-accumulate module comprising:  
2 a multiply-accumulate core, wherein said multiply-accumulate  
3 core comprises:  
4 a plurality of Booth encoder cells;  
5 a plurality of Booth decoder cells connected to at least  
6 one of said Booth encoder cells, said plurality of Booth decoder  
7 cells including at least one first Booth decoder cell and at least  
8 one second Booth decoder cell, said at least one first Booth  
9 decoder cell structurally the same as said at least one second  
10 Booth decoder cells; and  
11 a plurality of Wallace tree cells connected to at least  
12 one of said Booth decoder cells, said plurality of Wallace tree  
13 cells including at least one first Wallace tree cell and at least  
14 one second Wallace tree cell, said at least one first Wallace tree  
15 cell structurally the same as said at least one second Wallace tree  
16 cell;  
17 wherein said multiply-accumulate module includes at least one  
18 critical path, a critical path being an electrical path for which  
19 an amount of time that it takes for an electrical signal to travel  
20 from an input of said multiply-accumulate core to an output of said  
21 multiply-accumulate core is greater than or equal to a  
22 predetermined amount of time, wherein said predetermined amount of  
23 time is less than a longest amount of time that it takes any other  
24 electrical signal to travel from said input of said multiply-  
25 accumulate core to said output of said multiply-accumulate core;  
26 wherein said at least one first Wallace tree cell or said at  
27 least one first Booth decoder cell are disposed on said at least  
28 one critical path;

29        wherein said at least one second Wallace tree cell and said at  
30 least one second Booth decoder cell are not disposed on any of said  
31 at least one critical path;

32        wherein said at least one first Wallace tree cell or said at  
33 least one first Booth decoder cell comprises a first plurality of  
34 transistors, and at least one second Wallace tree cell or at least  
35 one second Booth decoder cell comprises a second plurality of  
36 transistors, ~~wherein at least one critical path of said multiply-~~  
37 ~~accumulate module comprises said at least one first cell;~~ and

38        a width of at least one of said first plurality of transistors  
39 is greater than a width of ~~at least~~ a corresponding one of said  
40 second plurality of transistors.

2.        (Canceled)

1        3.        (Currently Amended) The multiply-accumulate module of claim 1,  
2 wherein said multiply-accumulate core further comprises:

3        an adder connected to at least one of said Wallace tree cells;  
4        a saturation detector connected to said adder, wherein said  
5 multiply-accumulate module further comprises:

6        at least one input register connected to at least one of said  
7 Booth encoding cells; and

8        at least one result register connected to said saturation  
9 detector, ~~wherein said critical path is an electrical path for~~  
10 ~~which an amount of time that it takes for an electrical signal to~~  
11 ~~travel from said at least one input register to said at least one~~  
12 ~~result register is greater than or equal to a predetermined amount~~  
13 ~~of time, wherein said predetermined amount of time is less than a~~  
14 ~~longest amount of time that it takes any other electrical signal to~~  
15 ~~travel from said at least one input register to said at least one~~  
16 ~~result register.~~

4 to 8. (Canceled)

9. (Original) The multiply-accumulate module of claim 1, wherein said at least one second cell is a most significant bit or a least significant bit and said at least one first cell is not a most significant bit or a least significant bit.

10. (Currently Amended) A parallel multiplier comprising:  
a parallel multiplier core, wherein said parallel multiplier core comprises:

a plurality of Booth encoder cells;

a plurality of Booth decoder cells connected to at least one of said Booth encoder cells, said plurality of Booth decoder cells including at least one first Booth decoder cell and at least one second Booth decoder cell, said at least one first Booth decoder cell structurally the same as said at least one second Booth decoder cells; and

a plurality of Wallace tree cells connected to at least one of said Booth decoder cells, said plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, said at least one first Wallace tree cell structurally the same as said at least one second Wallace tree cell;

wherein said multiply-accumulate module includes at least one critical path, a critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time, wherein said predetermined amount of time is less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core;

26        wherein said at least one first Wallace tree cell or said at  
27 least one first Booth decoder cell are disposed on said at least  
28 one critical path;

29        wherein said at least one second Wallace tree cell and said at  
30 least one second Booth decoder cell are not disposed on any of said  
31 at least one critical path;

32        wherein said at least one first Wallace tree cell or said at  
33 least one first Booth decoder cell comprises a first plurality of  
34 transistors, and at least one second Wallace tree cell or at least  
35 one second Booth decoder cell comprises a second plurality of  
36 transistors, ~~wherein at least one critical path of said parallel~~  
37 ~~multiplier comprises said at least one first cell;~~ and

38        a width of at least one of said first plurality of transistors  
39 is greater than a width of ~~at least~~ a corresponding one of said  
40 second plurality of transistors.

11. (Canceled)

1    12. (Currently Amended) The parallel multiplier of claim 10,  
2 wherein said parallel multiplier core further comprises:

3        an adder connected to at least one of said Wallace tree cells;  
4        a saturation detector connected to said adder, wherein said  
5 parallel multiplier further comprises:

6        at least one input register connected to at least one of said  
7 Booth encoding cells; and

8        at least one result register connected to said saturation  
9 detector and at least one of said Wallace tree cells, ~~wherein said~~  
10 ~~critical path is an electrical path for which an amount of time~~  
11 ~~that it takes for an electrical signal to travel from said at least~~  
12 ~~one input register to said at least one result register is greater~~  
13 ~~than or equal to a predetermined amount of time, wherein said~~  
14 ~~predetermined amount of time is less than a longest amount of time~~

15 ~~that it takes any other electrical signal to travel from said at~~  
16 ~~least one input register to said at least one result register.~~

13 to 17. (Canceled)

1 18. (Original) The multiply-accumulate module of claim 10, wherein  
2 at least one second cell is a most significant bit or a least  
3 significant bit and at least one first cell is not a most  
4 significant bit or a least significant bit.

1 19. (Currently Amended) A method of designing a multiply-  
2 accumulate module comprising the steps of:  
3 providing a multiply-accumulate core, wherein the step of  
4 providing a multiply-accumulate core comprises the steps of:  
5 providing a plurality of Booth encoder cells;  
6 connecting a plurality of Booth decoder cells to at least  
7 one of said Booth encoder cells;  
8 connecting a plurality of Wallace tree cells to at least  
9 one of said Booth decoder ~~eells,~~ cells;  
10 defining at least one critical path wherein said  
11 multiply-accumulate module, a critical path being an electrical  
12 path for which an amount of time that it takes for an electrical  
13 signal to travel from an input of said multiply-accumulate core to  
14 an output of said multiply-accumulate core is greater than or equal  
15 to a predetermined amount of time, wherein said predetermined  
16 amount of time is less than a longest amount of time that it takes  
17 any other electrical signal to travel from said input of said  
18 multiply-accumulate core to said output of said multiply-accumulate  
19 core;  
20 defining a Wallace tree cell disposed on said at least  
21 one critical path as a first Wallace tree cell;

22           defining a Wallace tree cell not disposed on any of said  
23 at least one critical path as second Wallace tree cell;  
24           defining a Booth decoder cell disposed on said at least  
25 one critical path as a first Booth decoder cell;  
26           defining a Booth decoder cell not disposed on any of said  
27 at least one critical path as second Booth decoder cell;  
28           ~~constructing each wherein at least one~~ first Wallace tree  
29 ~~cell or at least one~~ and each first Booth decoder cell ~~comprises of~~  
30 a first plurality of transistors, each first Wallace tree cell  
31 structurally the same as each second Wallace tree cell, and  
32 constructing each at least one second Wallace tree cell ~~or at least~~  
33 ~~one~~ and each second Booth decoder cell ~~comprises of~~ a second  
34 plurality of transistors, each first Booth decoder cell  
35 structurally the same as each second Booth decoder cell ~~wherein at~~  
36 ~~least one critical path of said multiply-accumulate module~~  
37 ~~comprises at least one first cell;~~  
38           selecting a first width for at least one of said first  
39 plurality of transistors; and  
40           selecting a second width for at least one of said second  
41 plurality of transistors which is less than said first width of a  
42 corresponding one of said first plurality of transistors.

1   20. (Currently Amended) A method of designing a parallel  
2 multiplier comprising the steps of:

3       providing a parallel multiplier core, wherein the step of  
4 providing a parallel multiplier core comprises the steps of:

5           providing a plurality of Booth encoder cells;

6           connecting a plurality of Booth decoder cells to at least  
7 one of said Booth encoder cells;

8           connecting a plurality of Wallace tree cells to at least  
9 one of said Booth decoder ~~cells,~~ cells;

10           defining at least one critical path wherein said  
11 multiply-accumulate module, a critical path being an electrical  
12 path for which an amount of time that it takes for an electrical  
13 signal to travel from an input of said multiply-accumulate core to  
14 an output of said multiply-accumulate core is greater than or equal  
15 to a predetermined amount of time, wherein said predetermined  
16 amount of time is less than a longest amount of time that it takes  
17 any other electrical signal to travel from said input of said  
18 multiply-accumulate core to said output of said multiply-accumulate  
19 core;

20           defining a Wallace tree cell disposed on said at least  
21 one critical path as a first Wallace tree cell;

22           defining a Wallace tree cell not disposed on any of said  
23 at least one critical path as second Wallace tree cell;

24           defining a Booth decoder cell disposed on said at least  
25 one critical path as a first Booth decoder cell;

26           defining a Booth decoder cell not disposed on any of said  
27 at least one critical path as second Booth decoder cell;

28           ~~constructing each wherein at least one~~ first Wallace tree  
29 ~~cell or at least one~~ and each first Booth decoder cell ~~comprises of~~  
30 a first plurality of transistors, each first Wallace tree cell  
31 structurally the same as each second Wallace tree cell, and  
32 ~~constructing each at least one~~ second Wallace tree cell ~~or at least~~  
33 ~~one and each~~ second Booth decoder cell ~~comprises of~~ a second  
34 plurality of transistors, each first Booth decoder cell  
35 structurally the same as each second Booth decoder cell ~~wherein at~~  
36 ~~least one critical path of said multiply-accumulate module~~  
37 ~~comprises at least one first cell;~~

38           selecting a first width for at least one of said first  
39 plurality of transistors; and

40            selecting a second width for at least one of said second  
41 plurality of transistors which is less than said first width of a  
42 corresponding one of said first plurality of transistors.